

REMARKS

Claims 1 – 60 are pending in the current application. Claims 1, 2, 13, and 21 have been amended. Claims 1- 4, 6, 7, 9 – 13, and 21 stand rejected, claims 5 and 8 stand objected to, and claims 14 – 20 and 28 – 60 are in condition for allowance. Applicant reserves the right to pursue the original claims and other claims in this and in other applications.

The Office Action states that formal drawings are required when the application is allowed. Applicant notes that formal drawings were submitted to the PTO on September 28, 2004.

Claim 2 stands rejected to under 35 U.S.C. 112, second paragraph. as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action states that claim 2 “is unclear and/or lacks antecedent basis. Correction/clarification is required.”

Claims 1 and 2 have been amended.

Claim 1 recites, inter alia, ramp generating circuitry comprising “an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage, said voltage control circuitry controlling application of a first voltage and a second voltage to each capacitance in said set, where said first voltage is higher than said second voltage.” (emphasis added)

Claim 2 recites, inter alia, the ramp generating circuitry according to claim 1 “in which the voltage control circuitry includes a multi-bit shift register with an output for each bit that controls whether said one of said respective first voltage and said second voltage is provided to a capacitance in said set.” (emphasis added)

As such, the lack of proper antecedent basis in claim 2 has been clarified and the rejection of claim 2 should be withdrawn.

Claims 1-3, 13, and 21-27 stand rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. Publication Number 2002/0122129) (“Lee”). Reconsideration is respectfully requested.

Lee discloses “an enhanced CMOS sensor improving picture quality by concurrently performing a gamma correction and an analog-to-digital conversion.” (Lee, Abstract)

With respect to claim 1, Lee fails to disclose or suggest “said voltage control circuitry controlling application of a first voltage and a second voltage to each capacitance in said set.” As such the rejection of claim 1 should be withdrawn.

Claims 2 and 3 depend from claim 1 and incorporate, directly or indirectly, the limitations thereof. Accordingly, withdrawal of the rejection of these claims is respectfully requested.

Claims 13 and 21 have been amended to include the same limitation that has been added to claim 1.

Claim 13 recites, *inter alia*, a ramp analog-to-digital (ADC) converter comprising “a ramp generator that includes: an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage; and ADC comparison circuitry that receives an analog input signal and said ramp signal of said combined output voltage, said ADC comparison circuitry providing a digital output signal indicating magnitude of said analog input signal, said voltage control circuitry controlling application of a first

voltage and a second voltage to each capacitance in said set, where said first voltage is higher than said second voltage.”

Claim 21 recites, inter alia, an imaging device comprising “an array of pixels; a signal processing circuit that receives analog signals from pixels in said pixel array and provides, for each analog signal, a corresponding digital signal; and ramp generating circuitry that provides a ramp signal to said signal processing circuitry, said ramp generating circuitry including: an array of capacitances, each with a first lead connected to provide a combined output voltage and a second lead; and voltage control circuitry connected to the second lead of each of a set of two or more capacitances in said array, said voltage control circuitry controlling a voltage on each of said set of capacitances to produce a ramp signal of said combined output voltage, said voltage control circuitry controlling application of a first voltage and a second voltage to each capacitance in said set, where said first voltage is higher than said second voltage.”

As such, the rejection of claims 13 and 21 should also be withdrawn for at least the reasons provided above.

Claims 22 -27 depend from claim 21 and incorporate, directly or indirectly, the limitations thereof. Accordingly, withdrawal of the rejection of these claims is respectfully requested.

Claims 4, 6-7, and 9-12 stand rejected under 35 U.S.C. 102(e) as being anticipated by Krymski et al. (U.S. Patent Number 6,476,751) (“751”) (“Krymski”). Reconsideration is respectfully requested.

Krymski discloses an “A-to-D converter system having programmed reference signal levels using only supply signal provided by a power supply.” (Krymski, Abstract)

Claim 4 recites, inter alia, a ramp generator comprising “a multi-bit shift register with a clock signal input, a reset signal input and, for each bit, an output; clock signal

circuitry that provides a clock signal to said shift register's clock signal input; reset signal circuitry that provides a reset signal to said shift register's reset signal input; an array of capacitors having a common top plate and each of said array of capacitors having a bottom plate switched sequentially to one of a low reference voltage and a high reference voltage in response to a respective shift register bit's output, a charge on each of said capacitors in said array added to a ramp output signal on said top plate in response to a value in said shift register."

Krymski fails to disclose or suggest, *inter alia*, "a multi-bit shift register." Although the Office Action states that the "latches" of Krymski are allegedly equivalent to the "multi-bit shift register" of the present invention, the Examiner provides nothing to support this allegation.

To the contrary, the analog-to-digital conversion process of Krymski uses a weighing process to determine the digital signal, comparing a reference value (from a ramp generator circuit) against the analog signal value. By using successive approximation, when the comparison decision is made, the reference value, i.e., the weight on the "scale," is the digital representation of the analog signal. The latches of Krymski are used to store bits that indicate which capacitors that are connected to the reference voltage. (Krymski, Col. 1, 50-51) If the comparison match is found, the digital representation of the analog signal value (which is stored in the latches) is read out from the latches. (Krymski, Col. 3, 50-55)

In the present application, an analog signal and a signal from a ramp generator are compared with a reference value. The multi-bit shift register, based on a clock input, controls sequentially switching the bottom of capacitors from a Vref-low to Vref-hi thereby controlling the signal provided by the ramp generator. (¶¶ 30-35) When a comparison decision is made, latches store the value from a counter (based on a clock signal), which is the digital value of the analog pixel signal. (¶¶ 30-35) Thus, the multi-bit shift register of the present invention and the latches of Krymski do not operate in the same way and are not equivalent. Therefore, the rejection of claim 4 should be withdrawn.

Claims 6-7 and 9 -12 depend from claim 4 and incorporate, directly or indirectly, the limitations thereof. Accordingly, withdrawal of the rejection of these claims is respectfully requested.

Claims 5 and 8 stand objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

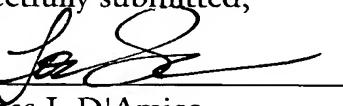
Claims 5 and 8 depend from claim 4 and incorporate, directly or indirectly, the limitations thereof and are allowable for at least the reasons stated above. Accordingly, withdrawal of the objection of these claims is respectfully requested.

The Applicant appreciates the allowance of claims 14 – 20 and 28 – 60.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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